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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,354	01/11/2002	Paul Matthew Carpenter	550-296	6802

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EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	4

DATE MAILED: 04/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,354	CARPENTER ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Claims 1-12 are presented for examination.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 6 recites the limitation "said sum of absolute differences" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulley et al. (USPN: 5,025,407) hereinafter, Gulley in view of Messina et al. (USPN: 4,317,168) hereinafter, Messina.

As per claim 1, Gulley teaches a data processing apparatus comprising a main processor (the graphics processor 120 in Fig. 1) responsive to program instructions to perform data processing operations and a coprocessor (the floating point coprocessor

1200 in Fig. 1) coupled to the main processor and responsive to a coprocessor load instruction (an instruction) on the main processor to load one or more loaded data words into the coprocessor and perform at least one coprocessor processing operation specified by the coprocessor load instruction using the one or more loaded data words to provide operand data to generate at least one result data word (e.g. see Col. 2, lines 3-10 and Fig. 1). However, Gulley does not teach that the number of loaded data words loaded into the coprocessor is depended upon whether or not the start address of the operand data is aligned with a word boundary.

Messina, on the other hand, teaches that the number of loaded data words (the quad words, QW) loaded (for the line fetch, LF) is depended upon the operand data alignment within the word boundary, i.e. 8 or 9 quad words (QW) occur for a line fetch (LF) depending upon the double word (DW) boundary alignment (e.g. see Abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the step of deciding whether to load one or more loaded data words based on the operand data alignment within the word boundary as taught by Messina in Gulley's apparatus. In doing so, the coprocessor load instruction gets the required number of operands and can start the execution of the load instruction without waiting for the remaining operands. Therefore, the number of clock cycles required for the execution of the coprocessor load instruction is reduced.

As per claims 11 and 12, Gulley teaches a method of processing data and a computer program product for controlling a computer comprising the steps of: in response to program instructions performing data processing operations in a main

processor (the graphics processor 120 in Fig. 1) and in response to a coprocessor load instruction (an instruction) on the main processor loading one or more loaded data words into a coprocessor (the floating point coprocessor 1200 in Fig. 1) coupled to the main processor and performing at least one coprocessor processing operation specified by the coprocessor load instruction using the one or more loaded data words to provide operand data to generate at least one result data word (e.g. see Col. 2, lines 3-10). However, Gulley does not teach that the number of loaded data words loaded into the coprocessor is depended upon whether or not the start address of the operand data is aligned with a word boundary.

Messina, on the other hand, teaches that the number of loaded data words (the quad words, QW) loaded (for the line fetch, LF) is depended upon the operand data alignment within the word boundary, i.e. 8 or 9 quad words (QW) occurred for a line fetch (LF) depending upon the double word (DW) boundary alignment (e.g. see Abstract). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the step of deciding whether to load one or more loaded data words based on the operand data alignment within the word boundary as taught by Messina in Gulley's method and computer program. In doing so, the coprocessor load instruction gets the required number of operands and can start the execution of the load instruction without waiting for the remaining operands. Therefore, the number of clock cycles required for the execution of the coprocessor load instruction is reduced.

4. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gulley in view of Messina further in view of York et al. (USPN: 6,002,881) hereinafter, York.

As per claim 2, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the coprocessor includes a coprocessor memory storing one or more locally stored data words used as operands in the at least one coprocessor processing operation in combination with the one or more loaded data words. York, on the other hand, teaches that the coprocessor (Piccono coprocessor 4 in Fig. 1) includes a coprocessor memory (registers 10 in Fig. 2) for storing one or more data words, which includes data words used as operands and loaded data words (emphasis added) (e.g. see Figs. 1-2 and Col. 5, lines 44-57). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the coprocessor memory in the coprocessor for storing locally stored data words along with the loaded data words as taught by York in Gulley and Messina's data processing apparatus. In doing so, the coprocessor retrieves these data words faster than storing it elsewhere (not locally to the coprocessor), which reduces the data latency and therefore, the performance of the coprocessor increases.

As per claim 3, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the data processing apparatus comprising a memory coupled to the main processor and wherein the one or more loaded data words are retrieved from the memory to the

coprocessor via the main processor without being stored within registers within the main processor. York, on the other hand, teaches a memory coupled to the main processor and wherein the one or more loaded data words are retrieved from the memory to the coprocessor via the main processor without being stored within registers within the main processor (e.g. see Col. 1, lines 18-34). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify the data processing apparatus taught by Gulley and Messina as such so the loaded data words can be retrieved from the memory to the coprocessor via the main processor without being stored within registers within the main processor as taught by York. In doing so, the data retrieval time reduces and therefore, the overall performance of the data processing apparatus increases.

As per claim 4, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the main processor includes a register operable to store an address value pointing to the one or more data words. York, on the other hand, teaches that the main processor (the CPU) includes a register, which holds an address value pointing to the data words (e.g. see Col. 2, lines 42-51). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Gulley and Messina's apparatus by adding an register in the main processor for storing an address value as taught by York so the start address within the memory to be accessed is determined.

As per claims 5 and 6, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that at least one coprocessor processing operation includes calculating a sum of absolute differences between a plurality of byte values within the one or more loaded data words and corresponding ones of a plurality of byte values within the one or more locally stored data words. York, on the other hand, teaches that one of the coprocessor processing operation (the SUBA instruction) calculates sum of differences (e.g. see Col. 36, lines 55-58). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Gulley and Messina's apparatus so the SUBA instruction can be run as taught by York. In doing so, the sum of differences between byte values within loaded and stored data words is calculated for the correlation purposes.

As per claim 7, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the sum of absolute differences is accumulated within an accumulate register of the coprocessor. York, on the other hand, teaches that sum of differences that calculated by the SUBA instruction is accumulated (added) in an accumulate register (the third register) (e.g. see Col. 36, lines 55-58). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Gulley and Messina's apparatus so the sum of differences is accumulated in the accumulate register as taught by York. In doing so, the sum of differences can be retrieved anytime by the coprocessor for any required manipulation. Since it is stored locally in the

coprocessor register, coprocessor can retrieve it quickly compare to if it is stored elsewhere.

As per claim 9, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the coprocessor load instruction includes an offset value to be added to the address value upon execution. York, on the other hand, teaches that the offset value (offset field within the instruction) is used by the CPU to specify the changes to be made in the address value provided by the CPU upon execution of a particular instruction (e.g. see the abstract and Col. 2, lines 42-51). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to modify Gulley and Messina's apparatus so upon the execution of an instruction, an offset that included in the instruction is added to the address value as taught by York. In doing so, the actual address is calculated from the given address value by adding an offset to that given address.

5. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulley in view of Messina further in view of Langendorf et al. (USPN: 4,860,197) hereinafter, Langendorf.

As per claim 8, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that the coprocessor includes an alignment register for storing a value specifying alignment between the operand data and the one or more loaded data words. Langendorf, on the other hand, teaches that the system includes one or more memory sets for storing

alignment values which represent whether the boundary of the instruction with one or more parcels (e.g. see the abstract and claim 6). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the alignment register for storing alignment value as taught by Langendorf in Gulley and Messina's apparatus so the required number of operands are loaded based on the alignment value and the execution of the load instruction is started without waiting for the remaining operands. Therefore, the number of clock cycles required for the execution of the coprocessor load instruction is reduced.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gulley in view of Messina further in view of Wu et al. (USPN: 6,418,166) hereinafter, Wu.

As per claim 10, the combination of Gulley and Messina teaches the claimed invention as described above. However, both Gulley and Messina failed to teach that at least one coprocessor processing operation calculates a sum of absolute differences as part of block pixel value matching. Wu, on the other hand, teaches that the sum of differences is used as the search criteria in the block matching process (e.g. see Fig. 8 and Col. 4, lines 42-44). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to use the sum of absolute differences as a part of block pixel value matching as taught by Wu in Gulley and Messina's apparatus. In doing so, it finds a block of pixels that most closely matches the source block of pixels. Therefore, it is advantageous.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is (703) 305-6219. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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